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said delay circuit and said programmable register being a single circuit and register connected to control the delay of said transmitter empty signal for each of said channels.

8. (Amended) The UART of claim 7 wherein said write-only register comprises the first 4 bits of a modem status register.

9. (Amended) The UART of claim 7 wherein said programmable register is a four bit register.

IN THE DRAWINGS:

The Examiner is requested is approve the drawing changes marked in red on the enclosed copy of Fig. 1.

REMARKS

Claims 1-10 are pending in this application. Claims 3, 4, and 7-9 have been amended. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Drawings.

The drawings are proposed to be amended, as requested by the Examiner, to add reference numbers for the blocks in Fig. 1 which did not have such reference numbers. In addition, the specification has been proposed to be amended to add a description of these blocks. Since the description merely recites the language found in the drawing itself, no new matter has been added. The Examiner is respectfully requested to approve the drawing changes.

Claims 3 and 7.

Claims 3 and 7 have been amended to address the Examiner's comment. In particular, the amendment specifies that there are two registers, which have the same address. This is believed to conform the claims to the comments of the Examiner and the

drawing in Fig. 4, as noted by the Examiner. The Examiner is thanked for the helpful comments in clarifying these claims.

Claims 8 and 9.

Claims 8 and 9 have been amended to change their dependency to claim 7. As noted by the Examiner, these claims as submitted were duplicates of claims 4 and 5 because they erroneously had the same dependency. This is believed to be corrected by this amendment.

Messerly.

Claim 1 has been rejected as anticipated by Messerly. It should be noted that Messerly is not directed to a UART as is the present invention, but rather to an interface between a UART and a host (digital signal processor, DSP). Messerly is directed to off-loading some of the handshaking and communication tasks that a host normally has to deal with in communicating with a UART.

The present invention, on the other hand, is directed to optimizing the timing between a UART and a host with circuitry inside the UART.

In particular, claim 1 sets forth a UART which comprises "a circuit for detecting a last word transmitted from said FIFO buffer." The office action compares this circuit to col. 4, lines 35-39 of Messerly. This portion of Messerly refers to a FIFO Fill Level Register. However, this register is located in the UART to DSP Interface (UDIF) 110 as is explained in col. 11, lines 48-65. Thus, Messerly does not show such a circuit as part of the UART, but rather as part of a separate interface. This has additional significance because of the different purpose of the interface as will be discussed in more detail below.

The office action similarly refers to the same language of Messerly with respect to the transmitter empty circuit of claim 1. Again, this is also not part of the UART as required by claim 1.

For the delay circuit of claim 1, the office action refers to col. 5, lines 16-24. This section of Messerly refers to a pacing wait count register which is also

described as a UDIF register. A similar description that it is a UDIF register is found in col. 11, line 61.

The purpose of these registers is different from that of the present invention as well. In the present invention, a delay is used to delay generation of the RTS signal to correspond to the time it will actually be leaving the UART chip, thus ensuring that the signal will be transmitted at the optimum time to both ensure that time is not wasted and that sufficient time is provided to avoid conflicts on the use of the serial bus.

In Messerly, on the other hand, there is no change to the output timing of the UART described at all. Rather, the interface device, the UDIF, builds in a delay so that it can mimic a UART connected directly to the host. This is described in col. 13, line 44 to col. 14, line 5. Finally, with respect to the programmable register, the office action refers to col. 6, lines 52-56 and col. 8, lines 14-17. These refer to the DIVL register, which is also in the UDIF, and not in the UART. (See col. 11, lines 54-55.) Again, as described in col. 13, line 44, *et seq.*, Messerly uses this to program a time which mimics the timing of the UART. It does not program a time which allows for a optimum generation of the signal from UART itself.

The remaining claims are believed distinguishable from Messerly for the same reasons. With respect to the shadow register described in claims 3, 4, 8 and 9, the office action additionally cites Tobias. Tobias describes a system which has different types of registers, including read-only, write-only and hidden registers. Tobias is concerned with storing data from these registers during periods of low-power hibernation. Nowhere, however, does Tobias suggest the advantages of using a shadow register to reduce the pin count for a UART chip. In addition, Tobias does not provide the recognition of the inventors of the present invention that the user does not need to be able to read back the programmable time written into the register, and thus a write-only register will serve the purpose of the present invention. Accordingly, these claims are believed distinguishable from the combination of Messerly and Tobias for these additional reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 3, the paragraph beginning at line 7, has been amended as follows:

Fig. 1 is a block diagram of a UART 10. The UART includes eight channels 12. Channel 0 indicates the internal circuitry for that channel, which is not shown but would be the same for the other eight channels. In particular, it has a 64-bit transmit first in/first out (FIFO) buffer 14 and a 64-byte receive FIFO 16. The channel also includes other control circuitry and registers. The channels interface via I/O lines 18 to serial data communication lines. The data can be provided through an internal bus 20 to an internal FIFO manager 22. The FIFO manager provides the data in both directions through a second internal bus 24 to a PCI local bus interface 26. This interfaces with a PCI bus 28. Fig. 1 also shows PCI bus configuration registers 13, an EEPROM interface 15, a 16-bit timer/counter 17, multipurpose inputs/outputs 19 and a crystal oscillator/buffer 21.

IN THE CLAIMS:

Claims 3, 4, and 7-9 have been amended as follows:

3. (Amended) The UART of claim 1 wherein said programmable register comprises a shadow register which is a write-only ~~portion of a~~ register with the same address as a read-only register only read by a user.

4. (Amended) The UART of claim 3 wherein said write-only ~~portion~~ register comprises the first 4 bits of a modem status register.

7. (Amended) A universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer;

a circuit for detecting a last word transmitted from said FIFO buffer;

a transmitter empty circuit for generating a transmitter empty signal on a transmitter empty control line when a last word transmitted from said FIFO buffer is detected, wherein said transmitter empty signal is an internal signal triggered from a stop bit of said last word;

a delay circuit for delaying generation of said transmitter empty signal for a programmable delay time;

a programmable register for setting said programmable delay time, wherein said programmable register comprises a shadow register which is a write-only ~~portion of a~~ register with the same address as a read-only register only read by a user;

a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and

said delay circuit and said programmable register being a single circuit and register connected to control the delay of said transmitter empty signal for each of said channels.

8. (Amended) The UART of claim ~~3~~ 7 wherein said write-only ~~portion~~ register comprises the first 4 bits of a modem status register.

9. (Amended) The UART of claim ~~1~~ 7 wherein said programmable register is a four bit register.

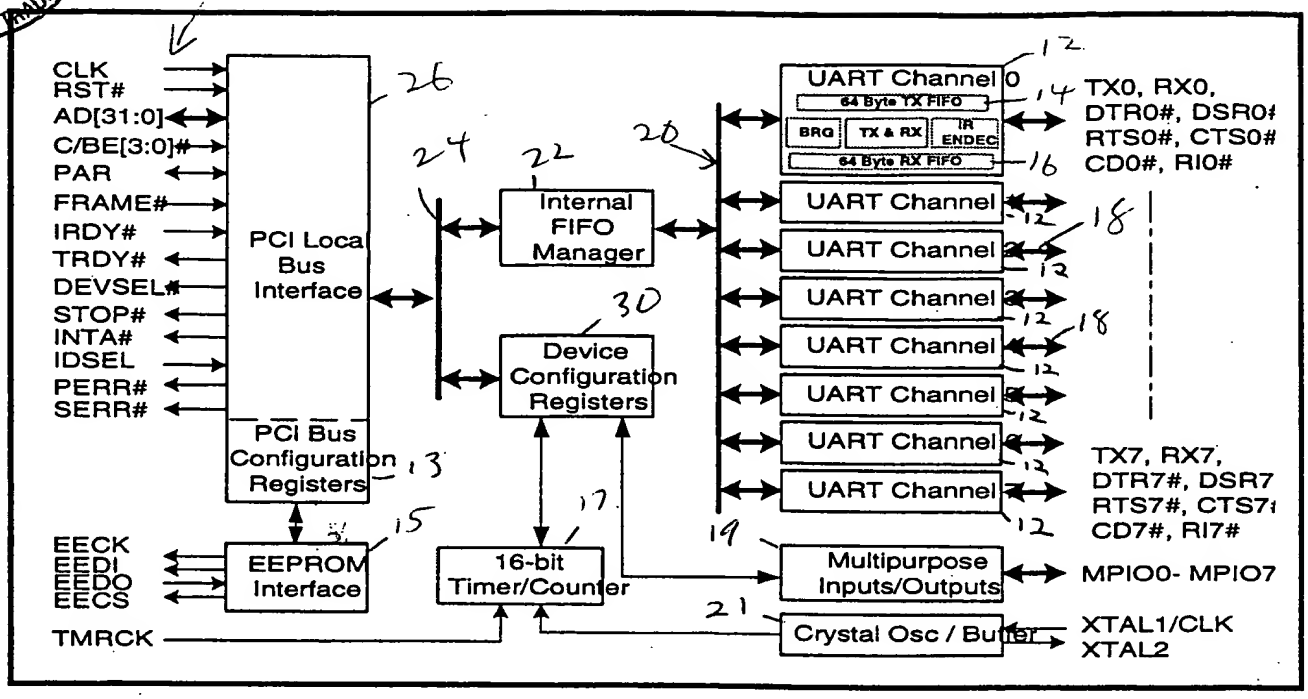

FIG. 1

Corrections approved by Examiner 2/14/03